

OB-U Type Ultra Low Phase Noise 2.5 x 2.0 mm SMD Differential Output Crystal Oscillator

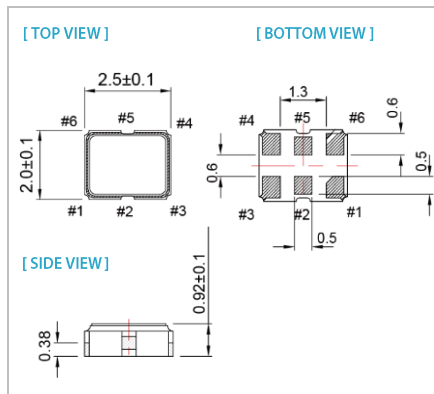
FEATURES

- Industry Standard 2.5 x 2.0 x 0.92mm Hermetically Sealed Ceramic Package
- Ultra Low Jitter Performance: Typical 50fs RMS from 12kHz - 20MHz
- Differential Output Level: LVPECL, LVDS and HCSL
- Operation Supply Voltage: 1.8V, 2.5V and 3.3V
- Pb-free/RoHS Compliant

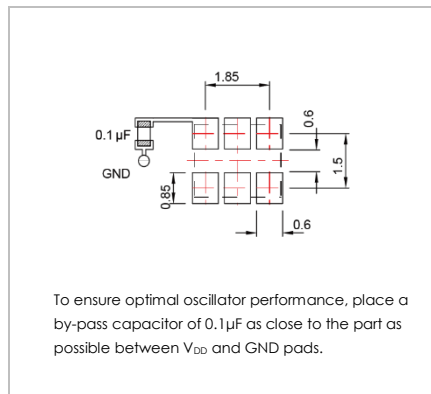
TYPICAL APPLICATION

- 40Gbit/100Gbit Ethernet, MAN, SONET, Fiber Channel
- Test Instrumentation

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



PIN FUNCTION (mm)

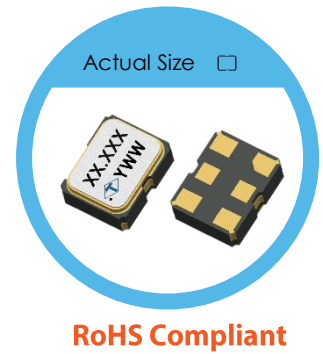
PIN#	FUNCTION
1	NC/Tri-State
2	Tri-State/NC
3	GND
4	Output
5	Comp. Output
6	V _{DD}

ELECTRICAL SPECIFICATION

Parameter		LVPECL				Unit	Test Condition
		3.3V		2.5V			
		Min.	Max.	Min.	Max.		
Supply Voltage Variation (V _{DD})		V _{DD} – 10%	V _{DD} + 10%	V _{DD} – 5%	V _{DD} + 5%	V	
Frequency Range		100	220	100	220	MHz	
Standard Frequency		100, 125, 156.25				MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			65		65	mA	
Output Level	Output High	2.215	2.42	1.415	1.64	V	
	Output Low	1.49	1.68	0.69	0.88	V	
Transition Time	Rise Time		0.4		0.4	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.4		0.4	nSec	
Duty Cycle		45	55	45	55	%	
Startup Time			5		5	mSec	
Tri-State	Enable	0.7 x V _{DD}		0.7 x V _{DD}		V	
	Disable		0.3 x V _{DD}		0.3 x V _{DD}	V	
Stand by Current			30		30	µA	
Output Loading		50Ω, V _{DD} – 2V					
RMS Phase Jitter Integrated 12 kHz~20 MHz @156.25MHz			0.1		0.1	pSec	
Aging (@ 25°C, First Year)			±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.		
At V _{DD} =3.3V, f _{out} =156.25MHz	10kHz offset	-150		-150		dBc/Hz	
	100kHz offset	-155		-155		dBc/Hz	
	1MHz offset	-160		-160		dBc/Hz	

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.



Parameter		LVDS						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V _{DD})		V _{DD} – 10%	V _{DD} + 10%	V _{DD} – 5%	V _{DD} + 5%	V _{DD} – 5%	V _{DD} + 5%	V	
Frequency Range		100	175	100	175	100	175	MHz	
Standard Frequency		100, 125, 156.25						MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			35		35		25	mA	
Output Level	Differential Output (V _{OD} , OUT-OUTN)	0.24	0.45	0.24	0.45	0.24	0.45	V	
	Output High		1.6		1.6		1.6	V	
	Output Low	0.9		0.9		0.9		V	
Transition Time	Rise Time		0.3		0.3		0.4	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.3		0.3		0.4	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			5		5		5	mSec	
Tri-State	Enable	0.7 x V _{DD}		0.7 x V _{DD}		0.7 x V _{DD}		V	
	Disable		0.3 x V _{DD}		0.3 x V _{DD}		0.3 x V _{DD}	V	
Stand by Current			30		30		30	μA	
Output Loading		100Ω (Between OUT & OUTN)						Ω	
RMS Phase Jitter Integrated 12 kHz~20 MHz @ 156.25MHz			0.1		0.1		0.1	pSec	
Aging (@ 25°C, First Year)			±3		±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V _{DD} =3.3V, f _{out} =156.25MHz	10kHz offset	-150		-150		-150		dBc/Hz	
	100kHz offset	-155		-155		-155		dBc/Hz	
	1MHz offset	-160		-160		-160		dBc/Hz	

Parameter		HCSL						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V _{DD})		V _{DD} – 10%	V _{DD} + 10%	V _{DD} – 5%	V _{DD} + 5%	V _{DD} – 5%	V _{DD} + 5%	V	
Frequency Range		100	135	100	135	100	135	MHz	
Standard Frequency		100, 125, 156.25						MHz	Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
Power Current Consumption			46		46		46	mA	
Output Level	Output High	0.6	0.9	0.6	0.9	0.5	1.0	V	
	Output Low	-0.15	0.15	-0.15	0.15	-0.15	0.15	V	
Transition Time	Rise Time		0.6		0.6		0.6	nSec	Transition times are measured between 20% and 80%
	Fall Time		0.6		0.6		0.6	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			5		5		5	mSec	
Tri-State	Enable	0.7 x V _{DD}		0.7 x V _{DD}		0.7 x V _{DD}		V	
	Disable		0.3 x V _{DD}		0.3 x V _{DD}		0.3 x V _{DD}	V	
Stand by Current			30		30		30	µA	
Output Loading		50 to GND						Ω	
RMS Phase Jitter Integrated 12 kHz~20 MHz @ 156.25MHz			0.1		0.1		0.1	pSec	
Aging (@ 25°C, First Year)			±3		±3		±3	ppm	
Storage Temp. Range		-55	125	-55	125	-55	125	°C	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V _{DD} =3.3V, f _{out} =156.25MHz	10kHz offset	-150		-150		-150		dBc/Hz	
	100kHz offset	-155		-155		-155		dBc/Hz	
	1MHz offset	-160		-160		-160		dBc/Hz	

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C)	ppm	± 20	± 25	± 50
-20 ~ +70		○	○	○
-40 ~ +85		△	○	○
-40 ~ +105		X	X	○
-40 ~ +125		X	X	△

○: Available △:Conditional x: Not Available
 Inclusive of calibration @ 25°C, operating temperature range,input Voltage variation,load variation,aging (1st year),shock,and vibration

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.